Atmel AT24CM01

I²C-Compatible (2-wire) Serial EEPROM
1-Mbit (131,072 x 8)

DATASHEET

Features

- Low voltage and standard voltage operation available
  - 1.7V (V_{CC} = 1.7V to 5.5V)
  - 2.5V (V_{CC} = 2.5V to 5.5V)
- Internally organized 131,072 x 8
- 2-wire serial interface
- Schmitt Triggers, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (5V, 2.5V) compatibility
- Write Protect pin for hardware data protection
- 256-byte Page Write mode
  - Partial page writes allowed
- Random and Sequential Read modes
- Self-timed write cycle (5ms max)
- High reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 40 years
- Green package options (Pb/Halide-free/RoHS Compliant)
  - 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, and 8-ball WLCSP
- Die sale options: wafer form and tape and reel available

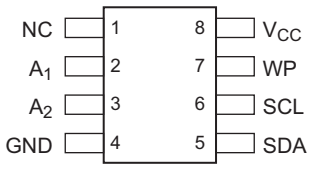
Description

The Atmel® AT24CM01 provides 1,048,576 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 131,072 words of eight bits each. The device's cascadable feature allows up to four devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, and 8-ball WLCSP. In addition, the entire family is available in 1.7V (1.7V to 5.5V) and 2.5V (2.5V to 5.5V) versions.

1. Pin Configurations and Pinouts

Pin Name	Function
NC	No Connect
A_1	Address Input
A_2	Address Input
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply

8-lead SOIC

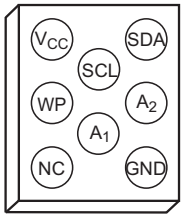


Top View

8-lead TSSOP

Top View

8-ball WLCSP



Bottom View

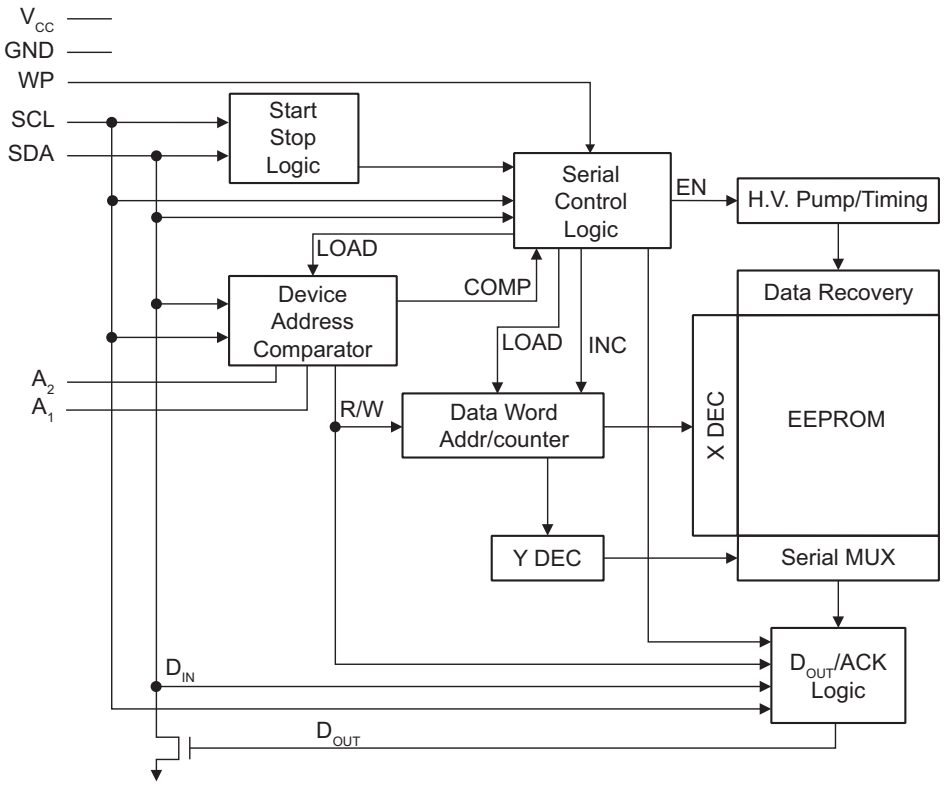
Note: Drawings are not to scale.

2. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open drain or open collector devices.

Device Addresses (A_2 and A_1): The A_2 and A_1 pins are device address inputs that can be hardwired or left not connected for hardware compatibility with other Atmel AT24Cxx devices. When the A_2 and A_1 pins are hardwired, as many as four 1-Mbit devices may be addressed on a single bus system (See “Device Addressing” on page 9 for more details). If the A_2 and A_1 pins are left floating, the A_2 and A_1 pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the A_2 and A_1 pin to GND.

Write Protect (WP): The Write Protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the pin to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Table 4-1. Write Protect

WP Pin Status	Part of the Array Protected
	AT24CM01
At V_{CC}	Full Array
At GND	Normal Read/Write Operations

5. Memory Organization

AT24CM01, 1-Mbit Serial EEPROM: The 1-Mbit is internally organized as 512 pages of 256 bytes each. Random word addressing requires a 17-bit data word address.

Table 5-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_2, A_1, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 5-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage, 1.7V Option			1.7		5.5	V
V_{CC2}	Supply Voltage, 2.5V Option			2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 400kHz			2.0	mA
I_{CC}	Supply Current	V_{CC} = 5.0V	Write at 400kHz			3.0	mA
I_{SB}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 2.5V				2.0	µA
		V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}			3.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level	V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 5-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V (where applicable), CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1300		400		ns
t_{HIGH}	Clock Pulse Width High	600		400		ns
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	50	900	50	550	ns
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1300		500		ns
$t_{HD.STA}$	Start Hold Time	600		250		ns
$t_{SU.STA}$	Start Set-up Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		300		300	ns
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	600		250		ns
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization only.

2. AC measurement conditions:
   - R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5V), 10 kΩ (1.7V)
   - Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   - Input rise and fall times: ≤ 50ns
   - Input and output timing reference voltages: 0.5 V_{CC}

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 6-4 on page 8). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command (see Figure 6-5 on page 8).

Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see Figure 6-5 on page 8).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in eight bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word (see Figure 6-6 on page 8).

Standby Mode: The AT24CM01 features a low power standby mode which is enabled:

- Upon power-up
- After the receipt of the stop bit and the completion of any internal operations

Software Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a start bit condition
2. Clock nine cycles
3. Create another start bit followed by stop bit condition as in Figure 6-1.

The device is ready for the next communication after above steps have been completed.

Figure 6-1. Software Reset

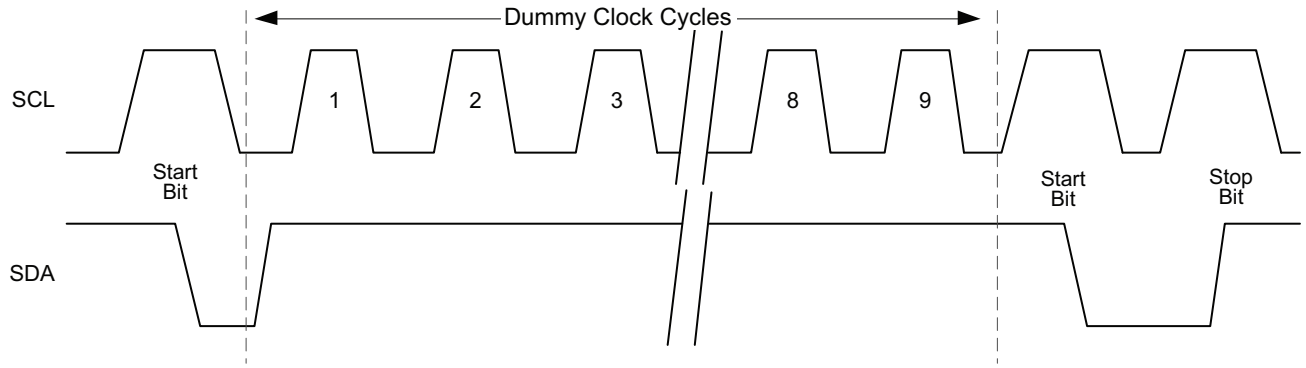


Figure 6-2. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

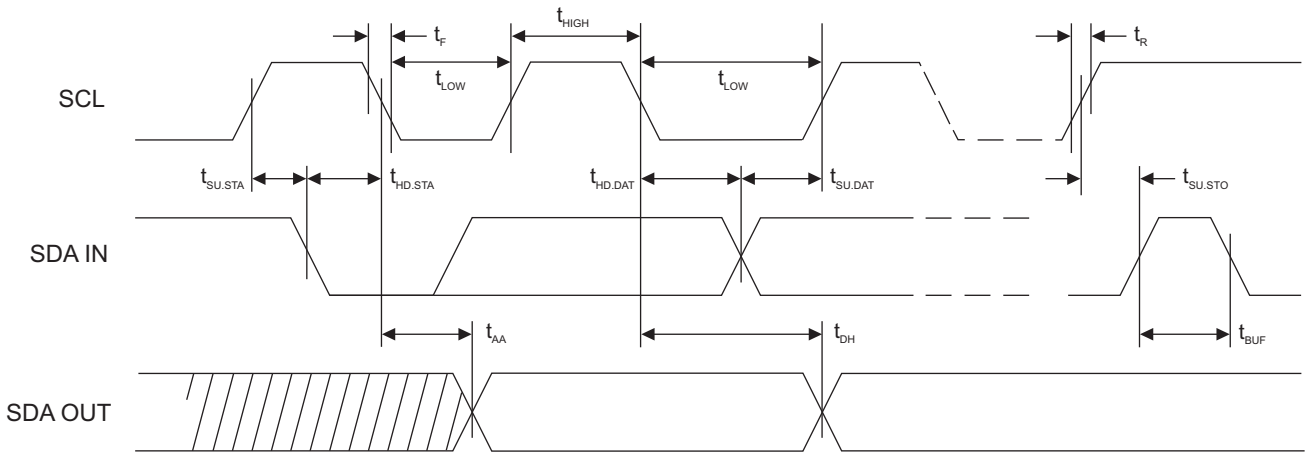
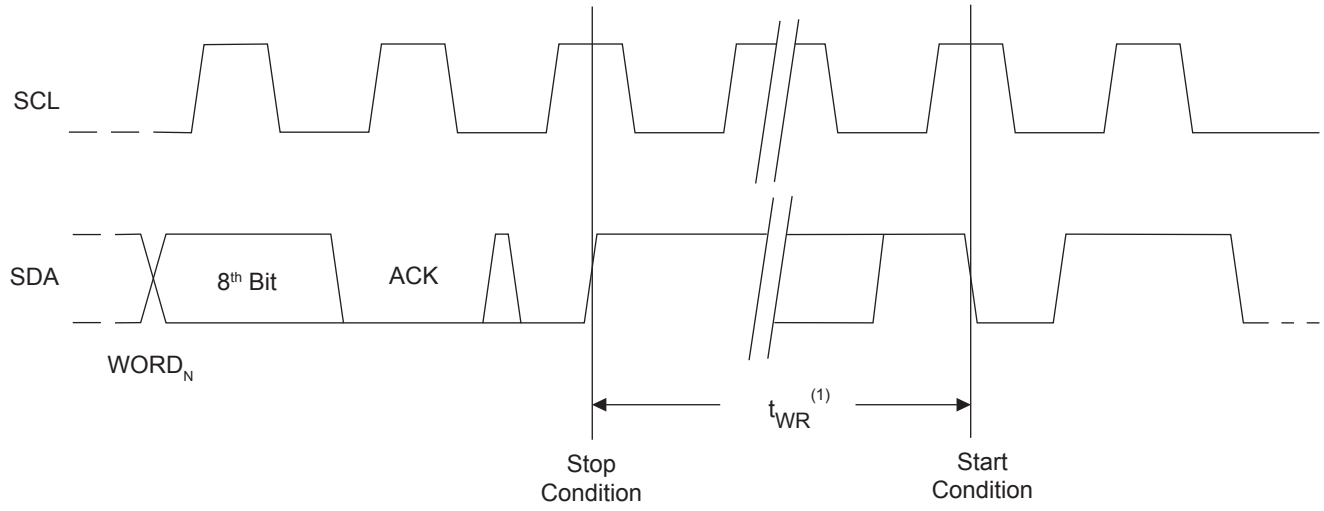


Figure 6-3. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



Notes: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 6-4. Data Validity

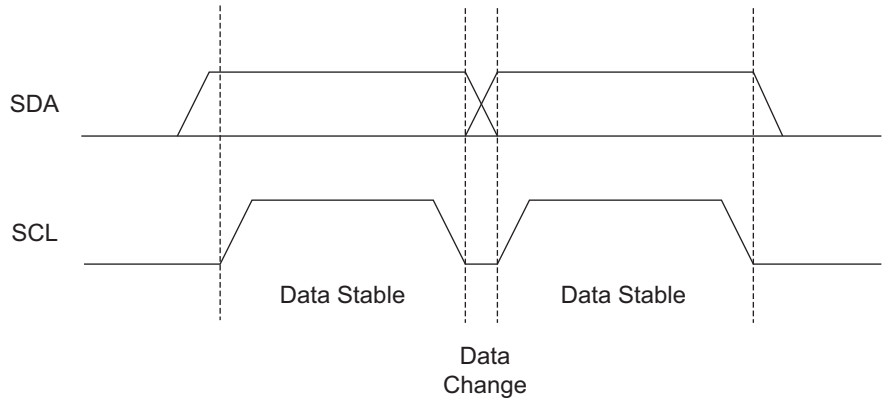


Figure 6-5. Start and Stop Definition

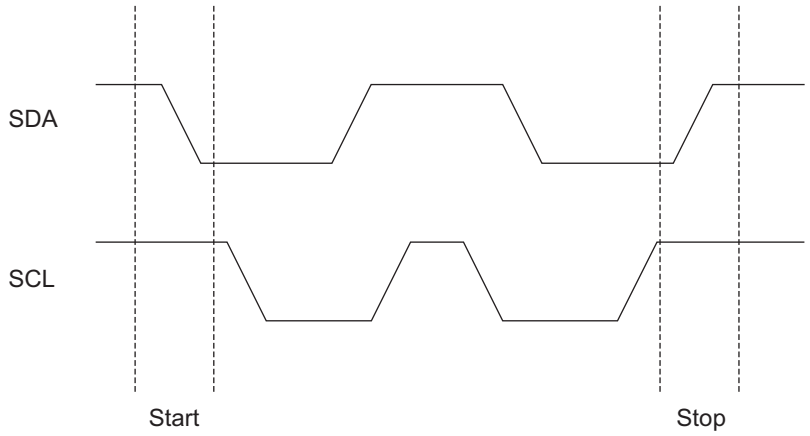
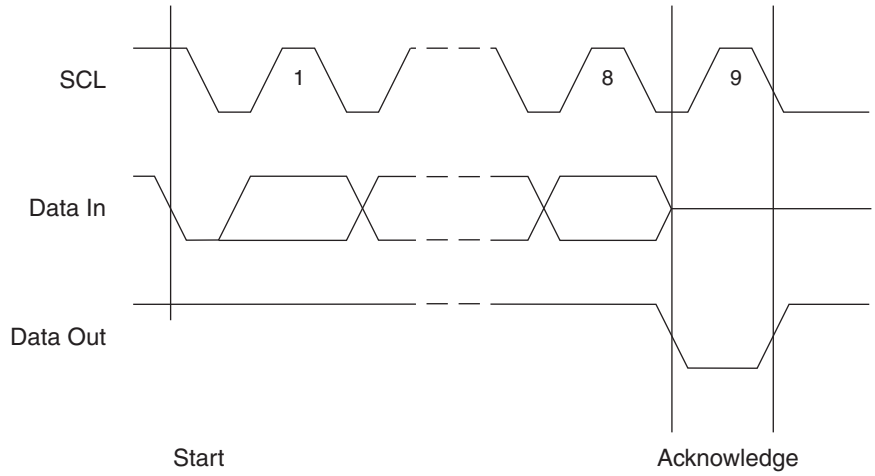


Figure 6-6. Output Acknowledge



7. Device Addressing

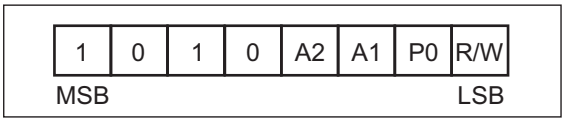
The 1-Mbit EEPROM requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation (see Figure 7-1 below). The device address word consists of a mandatory ‘1010’ sequence for the first four most significant bits. This is common to all 2-wire EEPROM devices.

The 1-Mbit uses the two device address bits, A2 and A1, to allow up to four devices on the same bus. These A2 and A1 bits must compare to the corresponding hardwired input pins, A_2 and A_1. The A_2 and A_1 pins uses an internal proprietary circuit that biases it to a logic low condition if the pin is allowed to float.

The seventh bit (P0) of the device address is a memory page address bit. This memory page address bit is the most significant bit of the data word address that follows. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a valid compare is not made, the device will return to a standby state.

Figure 7-1. Device Address

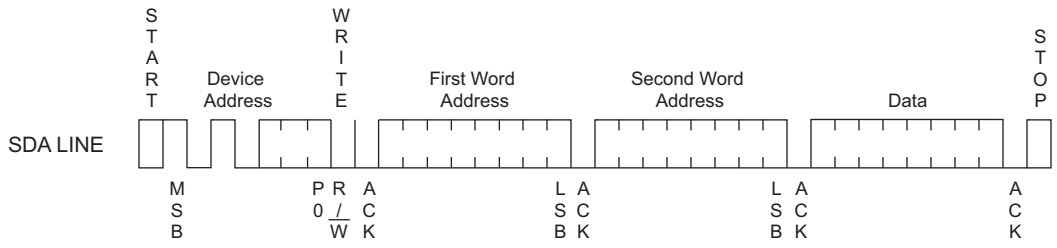


8. Write Operations

Byte Write: To select a data word in the 1-Mbit memory requires a 17-bit word address. The word address field consists of the P0 bit in the device address byte, then the most significant word address followed by the least significant word address (see Figure 8-1).

A write operation requires the P0 bit and two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then the part is to receive the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a Stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-1).

Figure 8-1. Byte Write

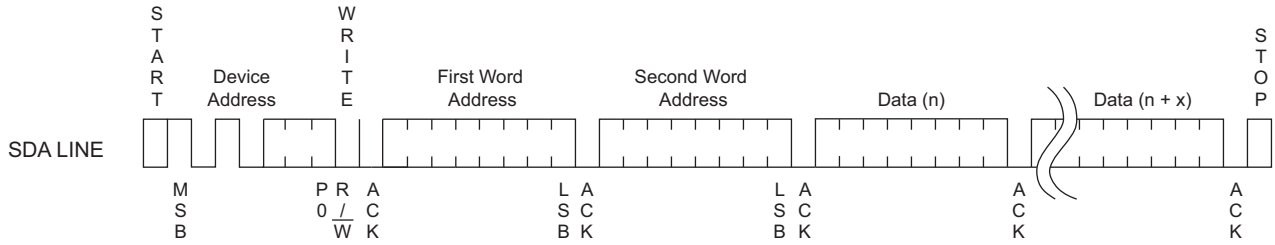


Page Write: The 1-Mbit EEPROM is capable of a 256-byte Page Write.

A Page Write is initiated the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 255 more data words. The EEPROM will respond with an acknowledge after each data word is received. The microcontroller must terminate the page write sequence with a Stop condition (see Figure 8-2) and the internally timed write cycle will begin.

The data word address lower 8 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “rollover” during write is from the last byte of the current page to the first byte of the same page.

Figure 8-2. Page Write



Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing a new read or write sequence to be initiated.

Data Security: The AT24CM01 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

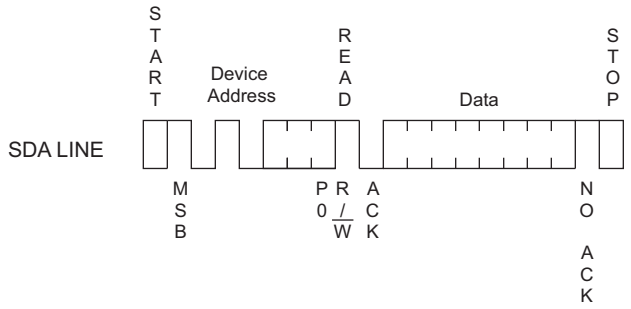
9. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: Current Address Read, Random Address Read, and Sequential Read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} to the part is maintained. The address “rollover” during read is from the last byte of the last page, to the first byte of the first page of the memory.

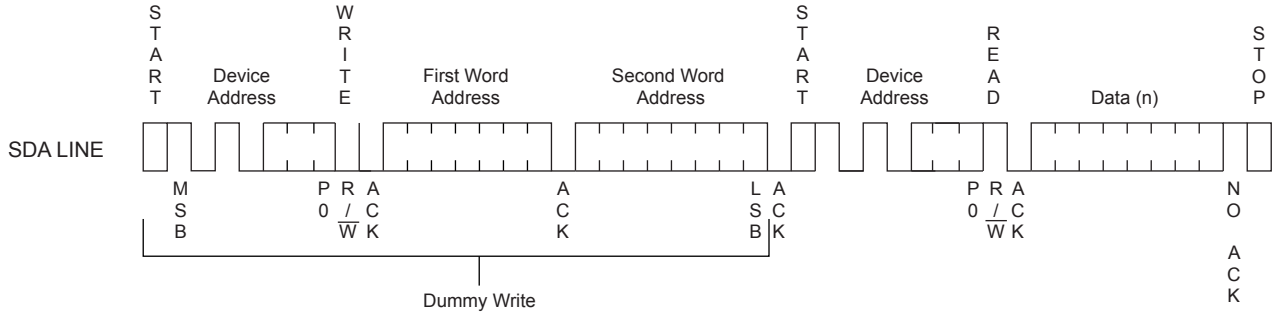
Once the device address with the read/write select bit set to one is input and acknowledged by the EEPROM, the current address data word is serially clocked out on the SDA line. The microcontroller does not respond with a zero but does generate a following Stop condition (see Figure 9-1).

Figure 9-1. Current Address Read



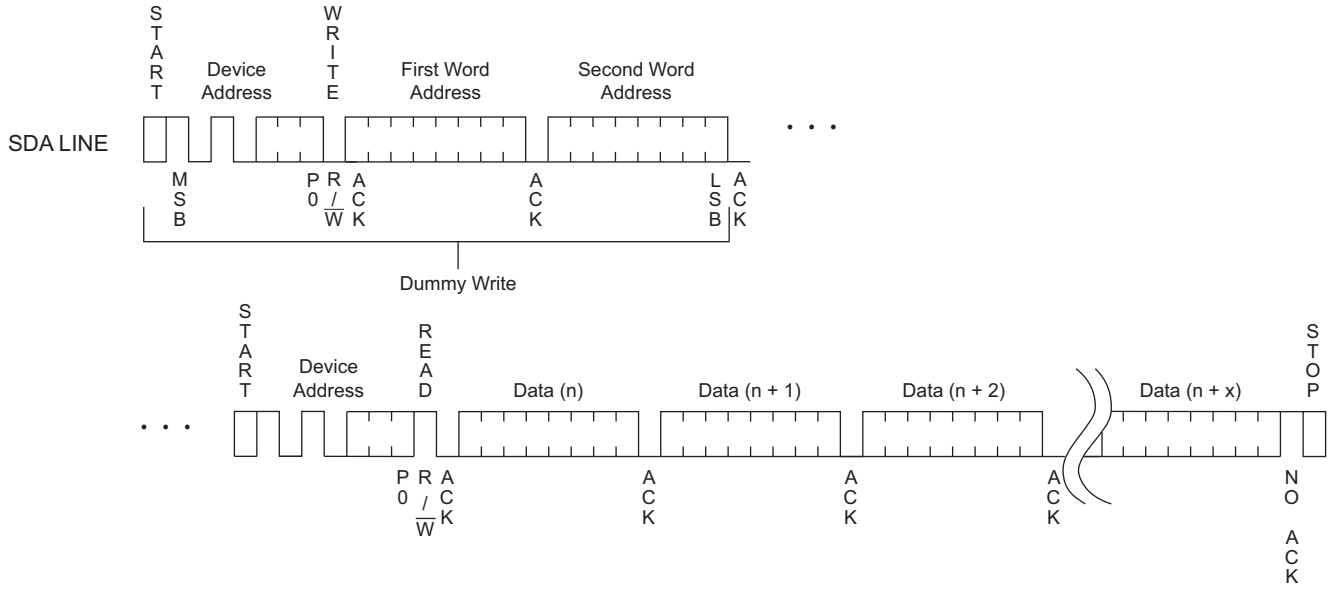
Random Read: A Random Read requires an initial byte write sequence to load in the data word address. This is known as a “dummy write” operation. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word on the SDA line. The microcontroller does not respond with a zero but does generate a following Stop condition (see Figure 9-2).

Figure 9-2. Random Read

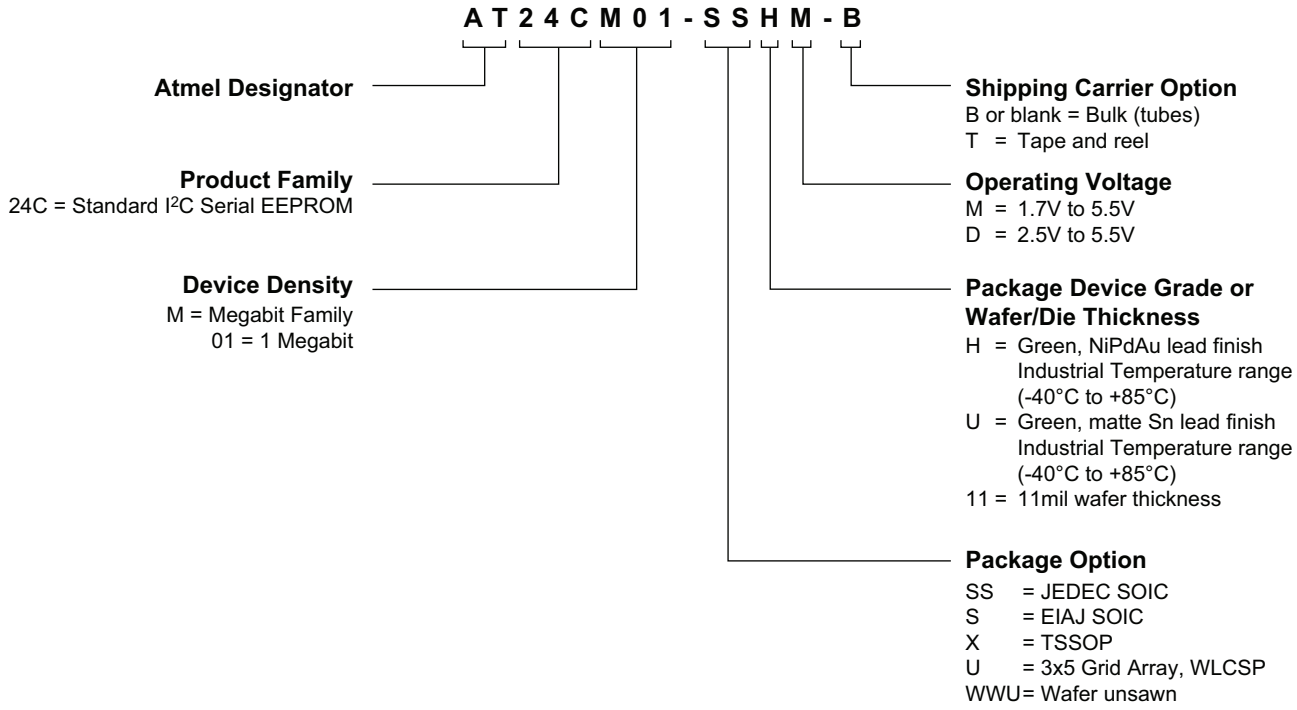


Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero, but does generate a following Stop condition (see Figure 9-3).

Figure 9-3. Sequential Read

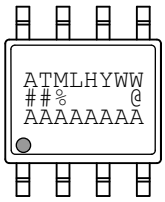
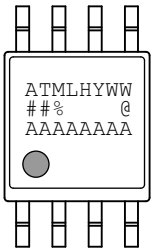
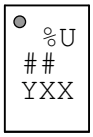


10. Ordering Code Detail



11. Part Markings

AT24CM01: Package Marking Information

8-lead SOIC	8-lead EIAJ
	
8-lead TSSOP	**8-ball WLCSP**
	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation		
AT24CM01	Truncation Code ##: 2G	
Date Codes		**Voltages**
Y = Year	WW = Work Week of Assembly	% = Minimum Voltage
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min D: 2.5V min
Country of Assembly	**Lot Number**	**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number	H: Industrial/NiPdAu U: Industrial/Matte Tin
		Atmel Truncation
		AT: Atmel ATML: Atmel

3/21/2013

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24CM01SM, AT24CM01 Package Marking Information	24CM01SM	F

12. Ordering Information

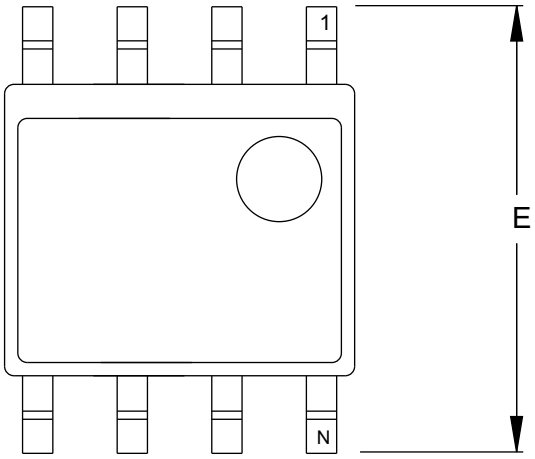
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT24CM01-SSHM-B[1]	NiPdAu (Lead-free/Halogen-free)	8S1	1.7V to 5.5V	Industrial Temperature (–40°C to 85°C)
AT24CM01-SSHM-T[2]				
AT24CM01-SSHD-B[1]			2.5V to 5.5V	
AT24CM01-SSHD-T[2]				
AT24CM01-SHM-B[1]		8S2	1.7V to 5.5V	
AT24CM01-SHM-T[2]				
AT24CM01-SHD-B[1]			2.5V to 5.5V	
AT24CM01-SHD-T[2]				
AT24CM01-XHM-B[1]		8X	1.7V to 5.5V	
AT24CM01-XHM-T[2]				
AT24CM01-XHD-B[1]			2.5V to 5.5V	
AT24CM01-XHD-T[2]				
AT24CM01-UUM-T	SnAgCu (Lead-free/Halogen-free)	8U-6	1.7V to 5.5V	
AT24CM01-WWU11M[3]	—	Wafer Sale		

Notes:
1. B = Bulk delivery in tubes:
   - SOIC and TSSOP = 100 per tube
2. T = Tape and reel delivery:
   - JEDEC SOIC = 4K units per reel
   - EIAJ SOIC = 2K units per reel
   - TSSOP and WLCSP = 5K units per reel
3. For wafer sales, please contact Atmel Sales.

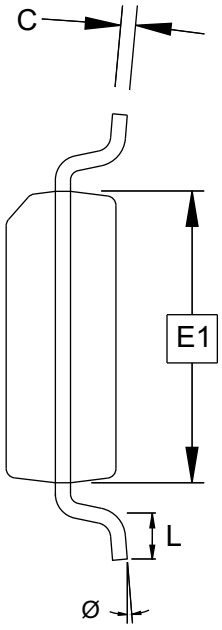
Package Type	
8S1	8-lead, 0.150” wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead, 0.208” wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8U-6	8-ball, 3x5 Grid Array, Wafer Level Chip Scale (WLCSP)

13. Packaging Information

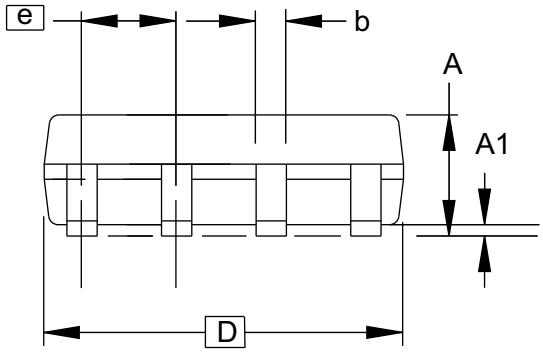
13.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

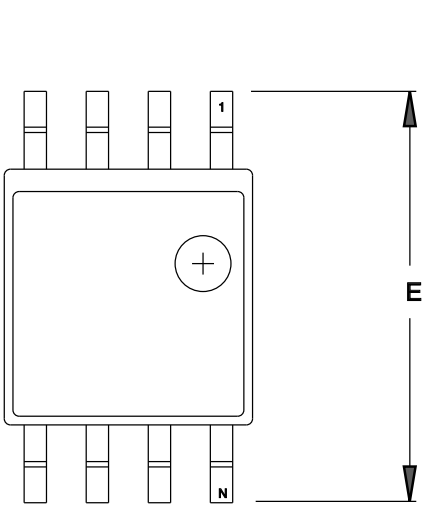
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

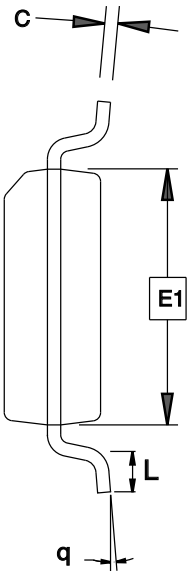
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

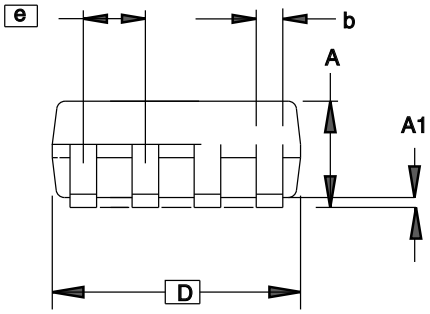
13.2 8S2 — 8-lead EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

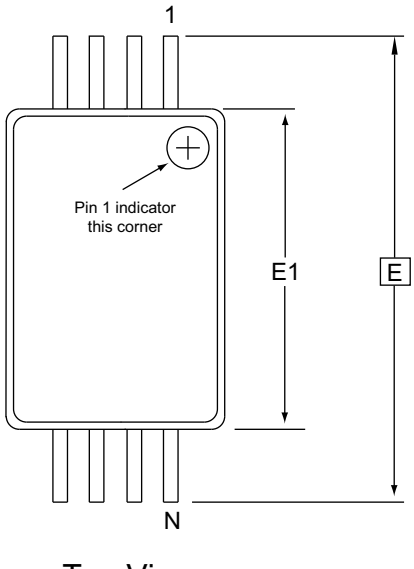
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
q	0°		8°	
e	1.27 BSC			3

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

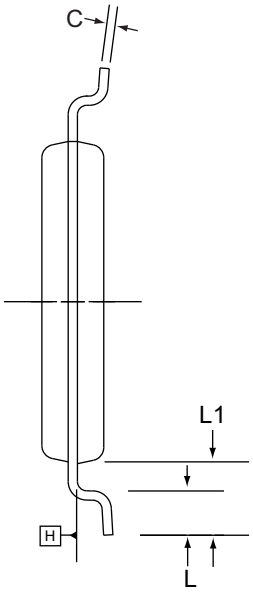
4/15/08

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **8S2,** 8-lead, 0.208” Body, Plastic Small Outline Package (EIAJ)	GPC STN	DRAWING NO. 8S2	REV. F

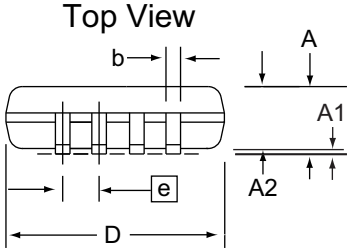
13.3 8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

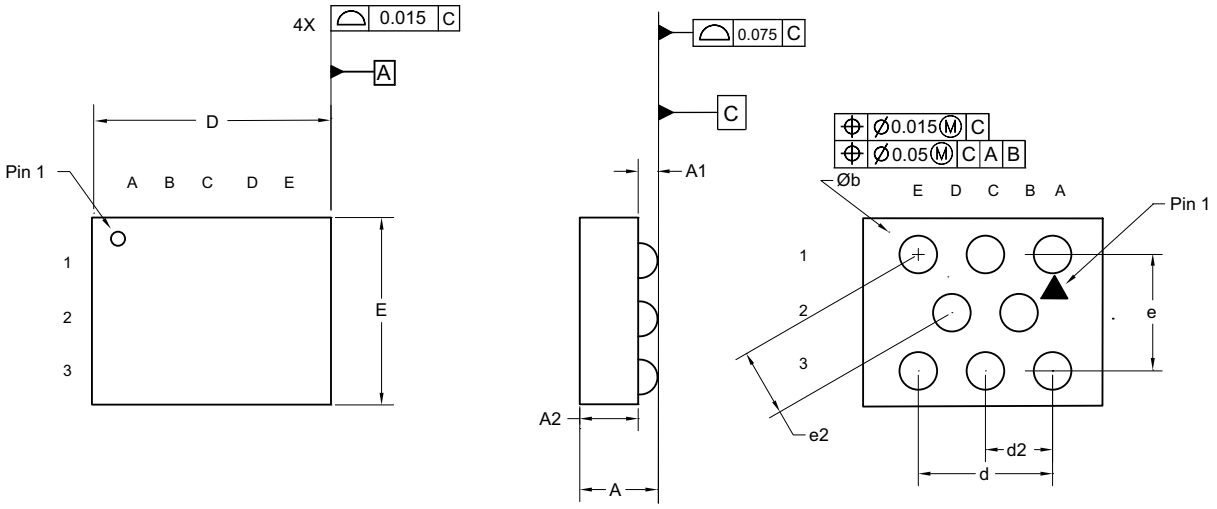
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

13.4 8U-6 — 8-ball WLCSP



TOP VIEW SIDE VIEW BALL SIDE

* Dimensions are NOT to scale.

PIN ASSIGNMENT MATRIX

	A	B	C	D	E
1	V_{CC}		WP		NC
2		SCL		A1	
3	SDA		A2		GND

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A			0.538	
A1	0.164	-	0.224	
A2	0.280	0.305	0.330	
E	Contact Atmel for details			
e		0.866		
e2		0.500		
d		1.000		
d2		0.500		
D	Contact Atmel for details			
b	0.239	0.269	0.299	

3/15/2013

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8U-6, 8-ball Wafer Level Chip Scale Package (WLCSP)	**GPC** GHZ	**DRAWING NO.** 8U-6	**REV.** B

14. Revision History

Doc. No.	Date	Comments
8821E	03/2013	Update document status from preliminary to complete. Correct WLCSP pinout. Update footers and disclaimer page.
8812D	01/2013	Correct TSSOP pin label 7 to WP.
8812C	12/2012	Add WLCSP package. Update part markings. Update pinout diagram. Update part markings. Correct Byte Write figure from second typo error to first word address. Update Sequential Read figure.
8812B	07/2012	Correct ordering code: - AT24CM01-WWU-11, Die Sale to AT24CM01-WWU11M, Wafer Sale. Update Atmel logos and disclaimer page.
8812A	05/2012	Initial document release.

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